Operation and Service Instructions LDMOS ALS-600 by CTR Engineering

Feb 2025 rev 1

This amplifier has been modified to use four MRF300 or equivalent FETs. The original TMOS MRF150 were the limiting factor. With MRF 300s the cooling, low pass filter, and the power supply become the new limiting factors. The primary reason to use MRF300 is FET life improvement, not power increase.

With 4x MRF300 power rating of this unit is now:

Maximum 300W average power during transmission periods longer than 60 seconds. This is limited by low pass filter, power supply, and heatsink temperature increase.

Maximum of 600W average RF power during any time period less than 30 seconds. This is limited by cooling airflow and the low pass filter component temperatures.

For example, 600W carrier for 30 seconds on and 30 seconds off for an extended time is okay. This would be 300W average and not exceed 600W. 600W or a little more power on normal CW will be fine.

800W PEP maximum envelope any period. This is limited by low pass filter peak voltage and power supply peak current. Avoid exceeding 800W PEP for any time period. The power supply and low pass filter will not like this.

Ratings typical summary:

FT8/ RTTY/ WSPR 600W 50% duty 30 second on max, 30 second off min
CW 600W+ normal CW
SSB 800W PEP any duty cycle

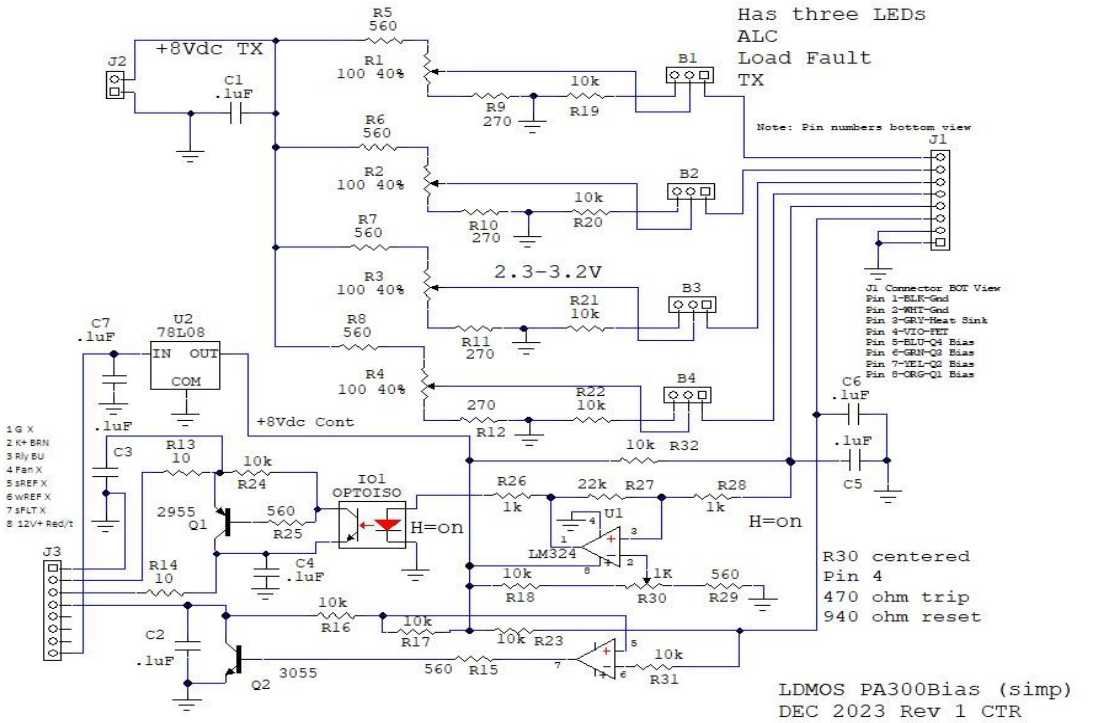
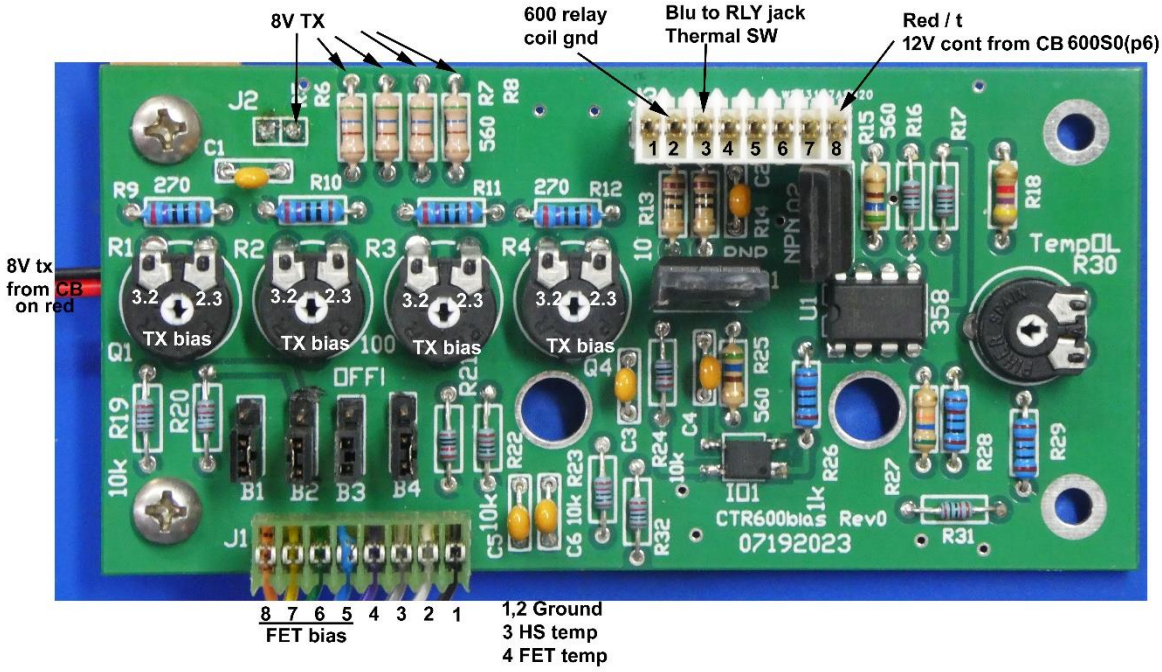


Figure 1 schematic bias

Bias Board

This amplifier has a new bias board. The bias board contains an FET temperature sensor. The thermal limit is set by R30. Full clockwise is most sensitive to FET heat. We recommend full clockwise, which is about 100* C.

The ideal bias is now 200-250 mA per FET or 800-1000 mA total with cold FETs. This is around 2.5 volts of gate bias but this must be set by monitoring FET current. To facilitate setting bias each FET has a three-pin shunt. These shunts are labeled B1 through B4. The shunts are moved away from the header J1 and toward the bias pots R1 through R4 to disable any or all FETs. By moving shunts and monitoring drain current, each FET can be set one FET at a time. Clockwise is maximum bias voltage and maximum FET current. Counter clockwise is minimum bias voltage and drain current. Each FET bias setting is independent of the other FETs.



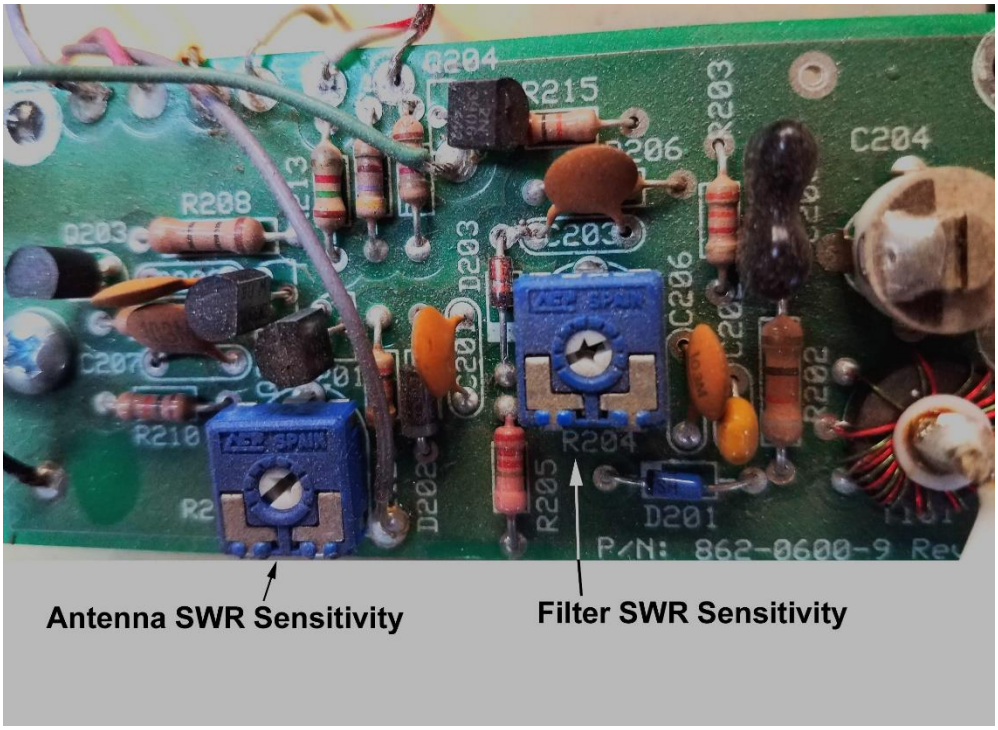


Figure 3 Existing Protections ALS600

PA Section

The new PA board uses two MRF300AN and two MRF300BN LDMOS. Nominal bias voltage is 2.5 Vdc. Drain supply voltage is 50 Vdc. The layout and schematic follow:

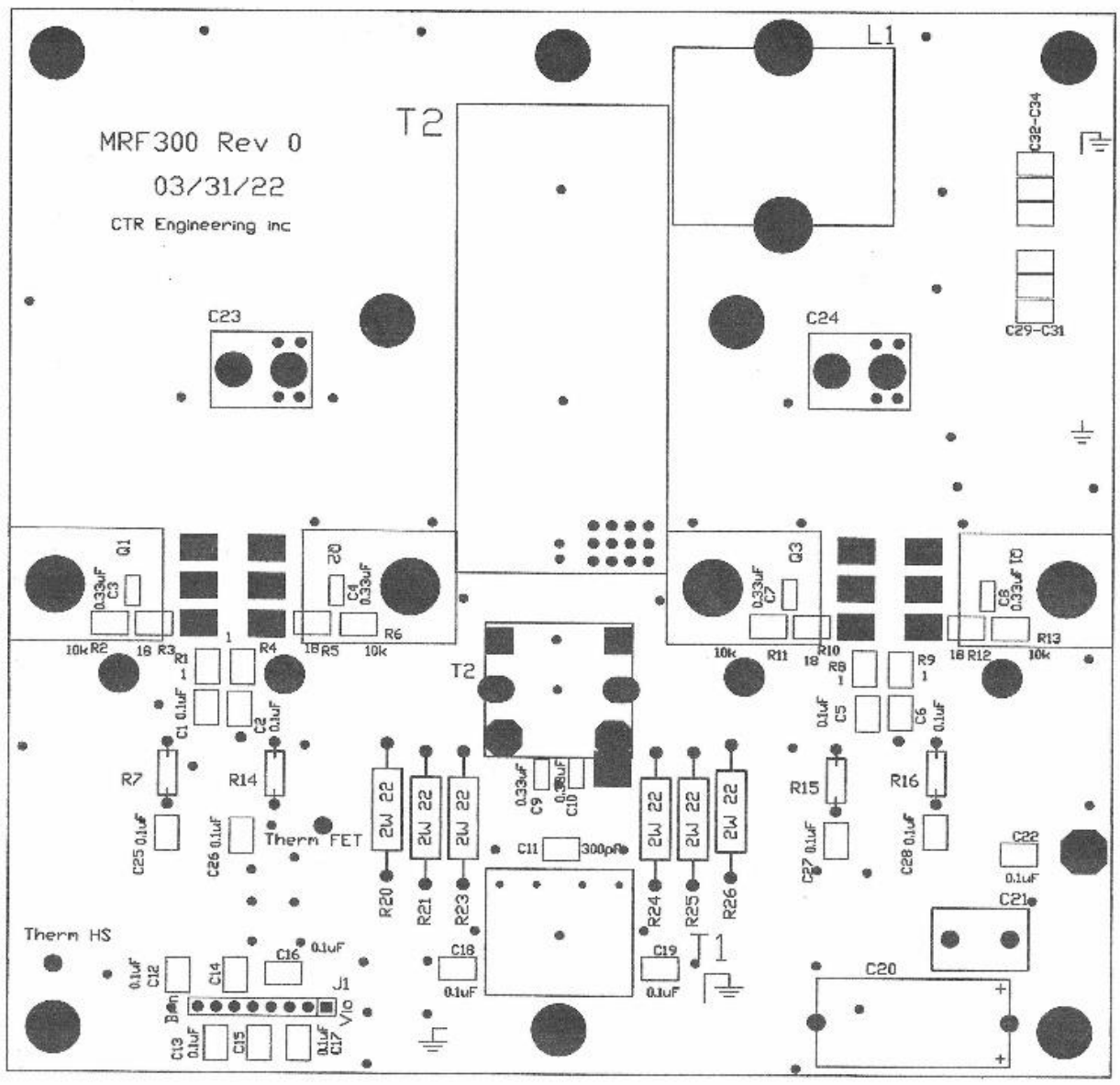


Figure 4 PA Layout

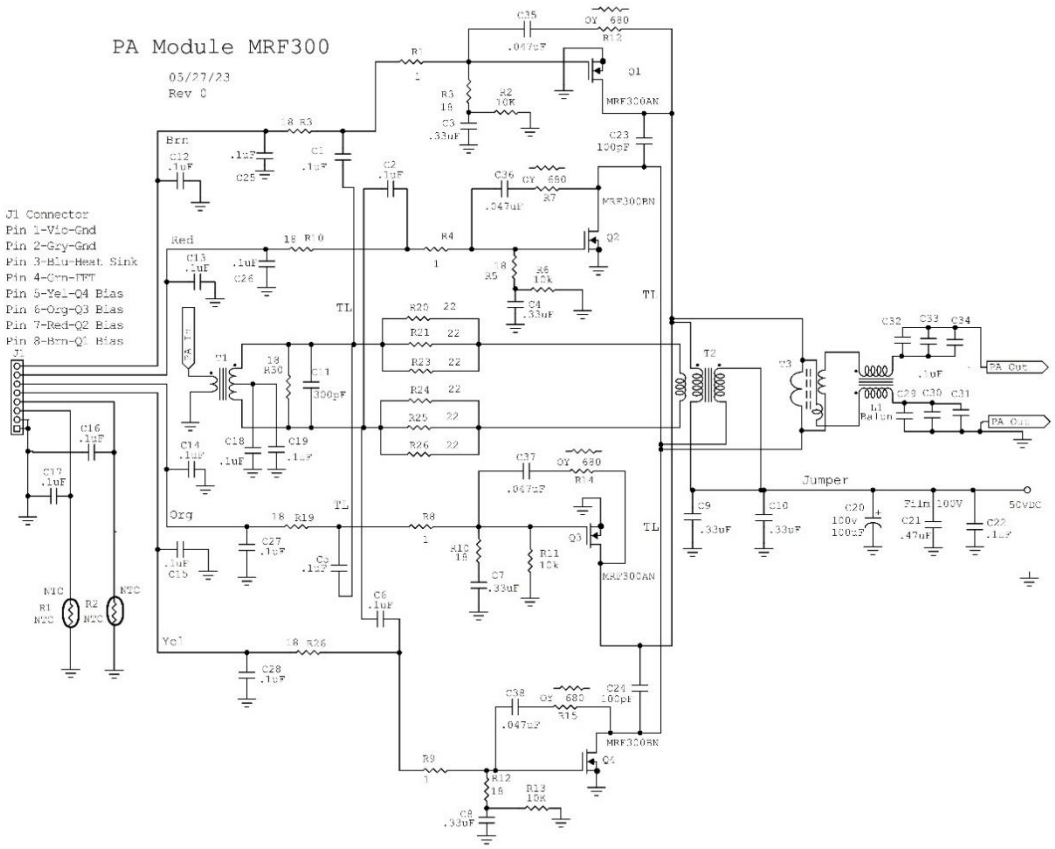


Figure 5 PA MRF300 LDMOS Schematic